1. A semiconductor wafer-in-process, comprising:

a substrate;

one or more global alignment sites located on a surface of said substrate, each said site including a global alignment mark;

a patterned layer of photoresist material on said substrate; and

a globule of protective material deposited over one or more said global alignment sites to protect said sites from an etching process using said patterned layer.

2. The wafer-in-process of claim 1, wherein said patterned layer of photoresist is over said global alignment sites.

3. The wafer-in-process of claim 2, wherein said globule of protective material is deposited over each global alignment site.

4. The wafer-in-process of claim 1, wherein said globule of protective material includes one or more from the group consisting of polymeric materials with photoactive elements, polymeric materials without photoactive elements, bottom anti-reflective coatings, spin-on glass materials, low dielectric constant materials, and polyimides.

5. The wafer-in-process of claim 1, comprising:

conductive patterning positioned immediately adjacent to said sites;

wherein said globule of protective material is also deposited over a portion of said conductive patterning for protecting said portion of conductive patterning from being etched.

6. A system for depositing protective material globules on a wafer-in-process comprising:

a protective material deposition device including:

a chamber adapted to receive and retain protective material; and

a nozzle extending from said chamber for dispensing the protective material; and

a base upon which the wafer-in-process is supported.

7. The system of claim 6, wherein said protective material deposition device is also capable of applying etching material to said wafer-in-process.

8. The system of claim 6, further comprising a vacuum source, wherein said nozzle includes a conduit for dispensing the protective material and an annulus, said annulus being in connection with said vacuum source.

9. The system of claim 8, wherein said vacuum source is adapted to pull excess protective material through said annulus.

10. A method of protecting one or more global alignment sites on a wafer from being etched, comprising:

coating the wafer with a photoresist material including over said global alignment sites;

exposing one or more portions of the photoresist material;

developing the exposed portions of the photoresist material including over said global alignment sites; and

depositing a protective material globule over one or more global alignment sites.

11. The method of claim 10, wherein said patterning of photoresist material comprises patterning the photoresist material over the global alignment sites by using full field images.

12. The method of claim 11, further comprising etching the wafer.

13. A method of protecting one or more feature structures during fabrication of a semiconductor wafer-in-process having a substrate, one or more global alignment sites, each having a global alignment mark, said method comprising:

depositing the feature structures at a position immediately adjacent to the global alignment sites; and

depositing a protective material globule over the global alignment mark and at least partially over the feature structures.

14. The method of claim 13, further comprising patterning a photoresist material over the global alignment sites before depositing said protective material.

15. The method of claim 14, wherein said patterning of photoresist material comprises patterning photoresist material over the global alignment sites by using full field images.

16. The method of claim 13, further comprising positioning one or more material layers over the global alignment marks.

17. The method of claim 13, further comprising removing a portion of the protective material globule.

18. The method of claim 17, wherein said removing step is accomplished through ashing.